Bab 3: Pengenalan TMS320C55x Digital Signal Processor

Dr. Ir. Yeffry Handoko Putra, M.T

© TemplatesWise.com

TMS320C5510 real-time DSP

- TMS320C55x family i: C5501, C5502, C5503, C5509, C5510,
- Features:
  - 64-byte instruction bekerja sebagai on-chip program cache
  - Dua 17-bit by17-bit MAC units dapat mengeksekusi operasi dual MAC operations pada satu siklus tunggal
  - Sebuah 40-bit arithmetic-and-logic unit (ALU) untuk high precision arithmetic dan 16-bit ALU untuk simple
  - Empat 40-bit accumulators
  - Dealapan extended auxiliary registers (XARs) untuk pengalamatan data dan 4 temporary data registers t
  - Circular addressing mode mendukung 5 circular buffers.
  - Single-instruction repeat and block-repeat operations untuk mendukung zero-overhead looping.
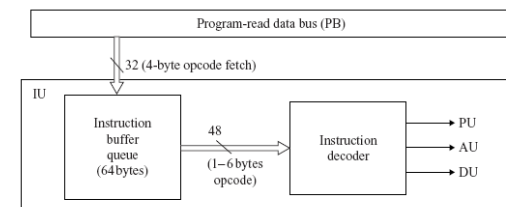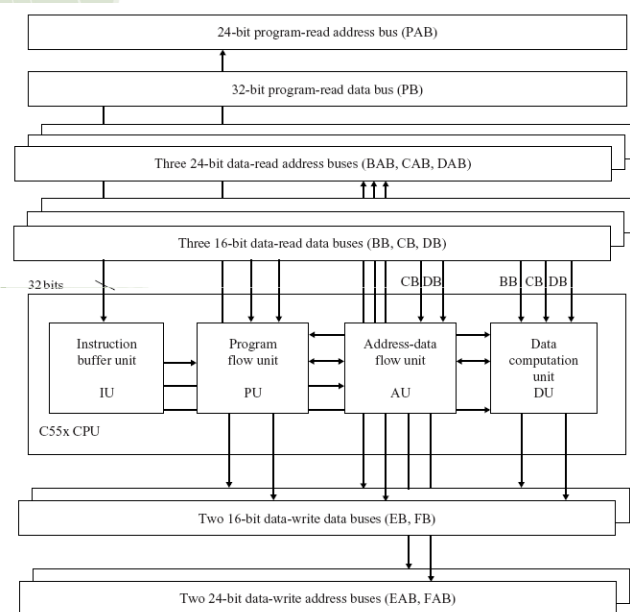

Arsitektur TMS320C55x

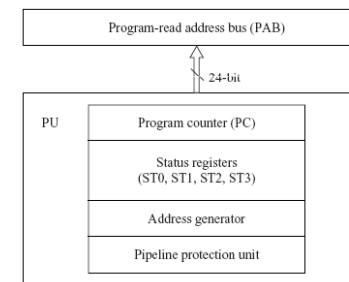Figure 2.2 Simplified block diagram of the C55x IU

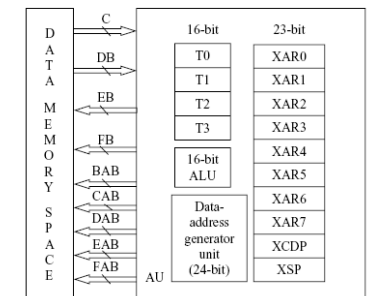Figure 2.3 Simplified block diagram of the C55x PU

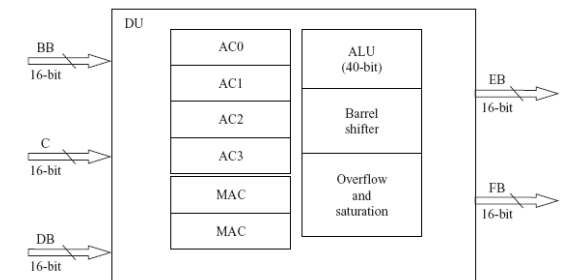Figure 2.4 Simplified block diagram of the C55x AU

Figure 2.5 Simplified block diagram of the C55x DU

4

Buses

- Jenis bus
  - 1 program data bus
  - 5 data buses
  - 6 address buses
- 32-bit PB and a 24-bit program-read address bus (PAB).
- Tiga 16-bit data-read data buses (BB, CB, and DB)
- Tiga 24-bit data-read address buses (BAB, CAB, and DAB)

On-Chip Memories

- C55x unified program and data memory configurations with separated I/O space. All 16 Mbytes of memory space are available for program and data.
- Ruang data memory digunakan untuk penyimpanan data. Memory mapped registers (MMRs) disisipkan pada data memory space.
- Saat processor melakukan fetching instructions dari memory digunakakan 24-bit PAB
  Saat prosesor mengakses memory digunakan jalur least significant bit (LSB) of the data address

Data space addresses (word in hexadecimal)	C55x memory program/data space	Program space addresses (byte in hexadecimal)
MMRs 00 0000–00 005F		00 0000–00 00BF Reserved
Page 0 { 00 0060 ... 00 FFFF		00 00C0 ... 01 FFFF
Page 1 { 01 0000 ... 01 FFFF		02 0000 ... 03 FFFF
Page 2 { 02 0000 ... 02 FFFF		04 0000 ... 05 FFFF
⋮	⋮	⋮
Page 127 { 7F 0000 ... 7F FFFF		FE 0000 ... FF FFFF

Figure 2.6   TMS320C55x program space and data space memory map

Table 2.1   C5510 DARAM blocks and addresses

DARAM byte address range	DARAM memory blocks
0x0000−0x1FFF	DARAM 0
0x2000−0x3FFF	DARAM 1
0x4000−0x5FFF	DARAM 2
0x6000−0x7FFF	DARAM 3
0x8000−0x9FFF	DARAM 4
0xA000−0xBFFF	DARAM 5
0xC000−0xDFFF	DARAM 6
0xE000−0xFFFF	DARAM 7

TMS320C55X ARCHITECTURE

Table 2.2   C5510 DARAM blocks and addresses

SARAM byte address range	SARAM memory blocks
0x10000−0x11FFF	SARAM 0
0x12000−0x13FFF	SARAM 1
0x14000−0x15FFF	SARAM 2
⋮	⋮
⋮	⋮
⋮	⋮
0x4C000−0x4DFFF	SARAM 30
0x4E000−0x4FFFF	SARAM 31

Memory Mapped Registers