

# **MATAKULIAH SISTEM DIGITAL**

## **PERTEMUAN XI**

### **COUNTER**

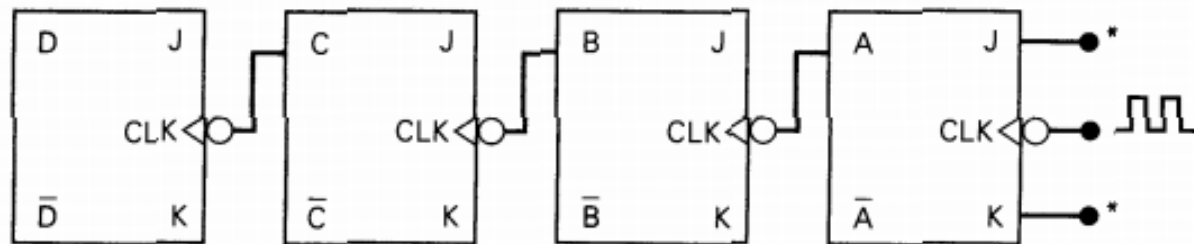
**OLEH :  
HIDAYAT**

**JURUSAN TEKNIK KOMPUTER  
UNIKOM  
2012**

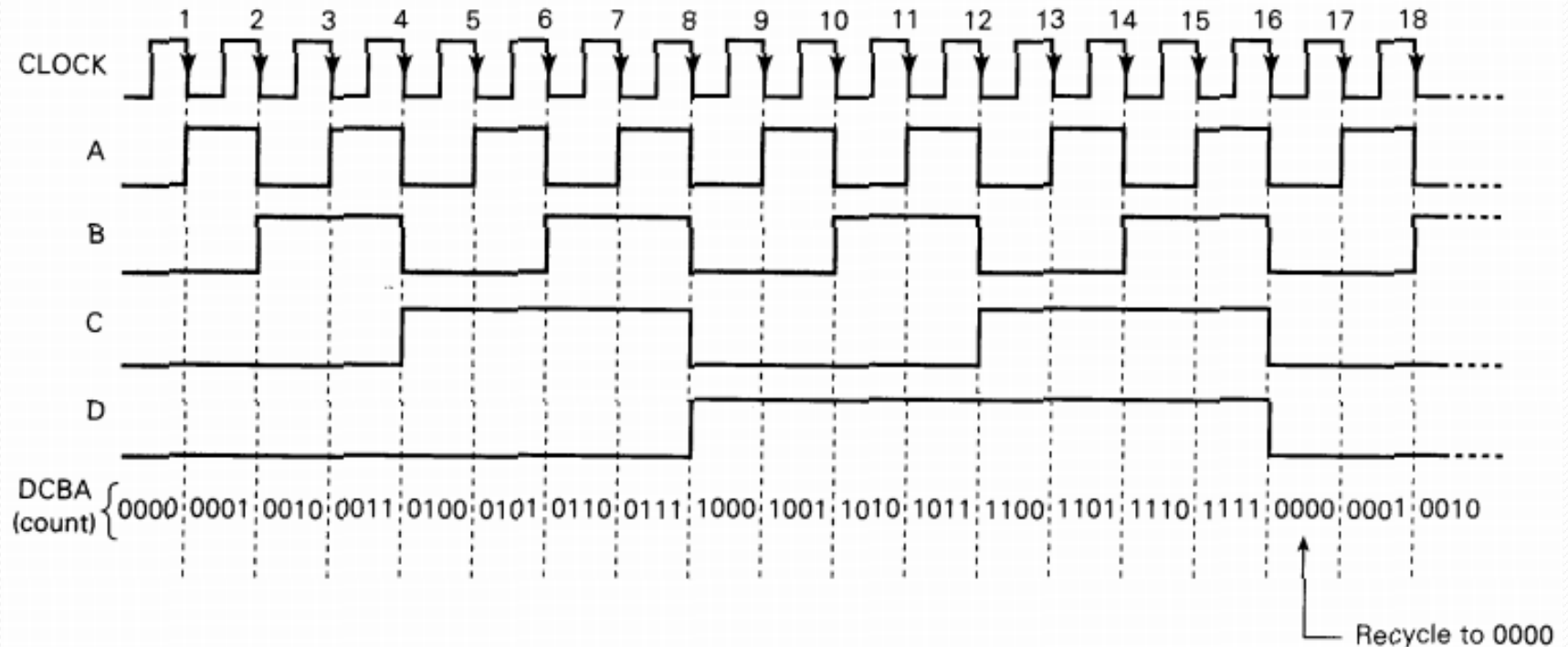
# Jenis

- Asynchronous (Ripple) Counter
- Synchronous Counter

# Asynchronous (Ripple) Counter



\*All J and K inputs  
assumed to be 1.



# Asynchronous (Ripple) Counter

- Pulsa clock hanya pada FF A,
- Semua nilai J dan K = 1
- Output normal FF A dijadikan input clock pada FF B, begitupun keluaran FF B dijadikan clock FF C dan seterusnya,
- Output D,C,B,A merepresentasikan 4 bit biner, D sbg MSB, A sbg LSB,
- Setelah nilai DCBA = 1111, pada clock berikutnya A toggle dari 1 menjadi 0, yang menyebabkan B toggle dari 1 menjadi 0, inipun menyebabkan C toggle dari 1 menjadi 0, dst, sehingga nilai DCBA menjadi 0000,
- Selanjutnya mengulangi pencacahan.

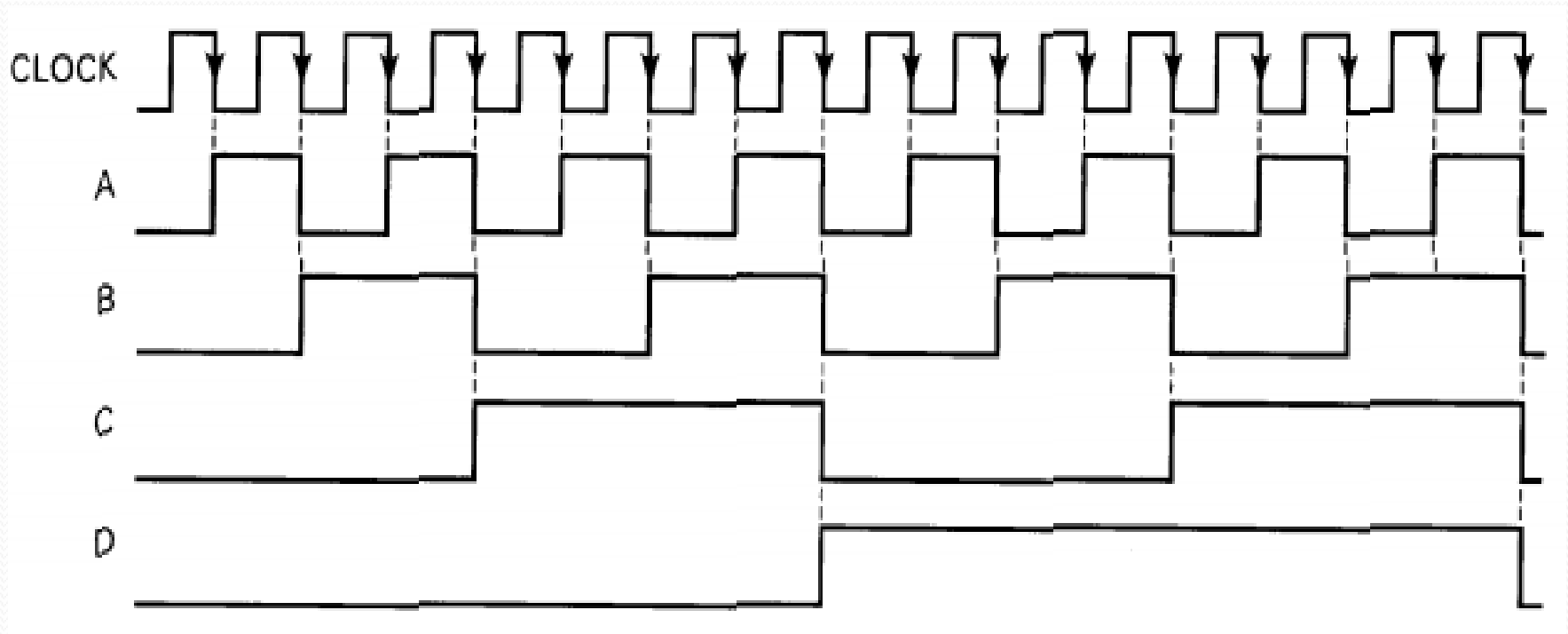
# Asynchronous Counter

- MOD number
  - Pencacah MOD  $2^N$  akan mencacah sejumlah  $2^N$
  - $N$  = banyaknya bit atau FF
  - Pencacah MOD  $N$  akan mencacah sejumlah  $N$

# Asynchronous Counter

- Pembagi Frekuensi

Contoh:



# Asynchronous Counter

- MOD 16 Counter
  - Output pada FF pertama adalah  $1/2$  frek. clock
  - Output pada FF kedua adalah  $1/4$  frek. clock
  - Output pada FF ketiga adalah  $1/8$  frek. clock
  - Output pada FF terakhir adalah  $1/16$  frek. clock
- MOD 8 Counter  $\rightarrow$  output =  $1/8$  frek. clock

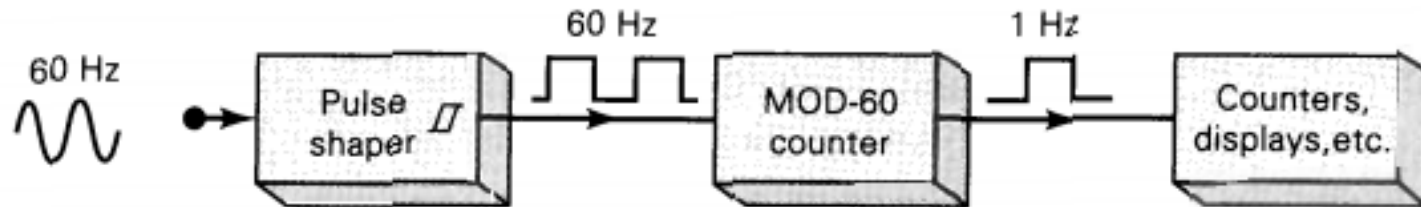
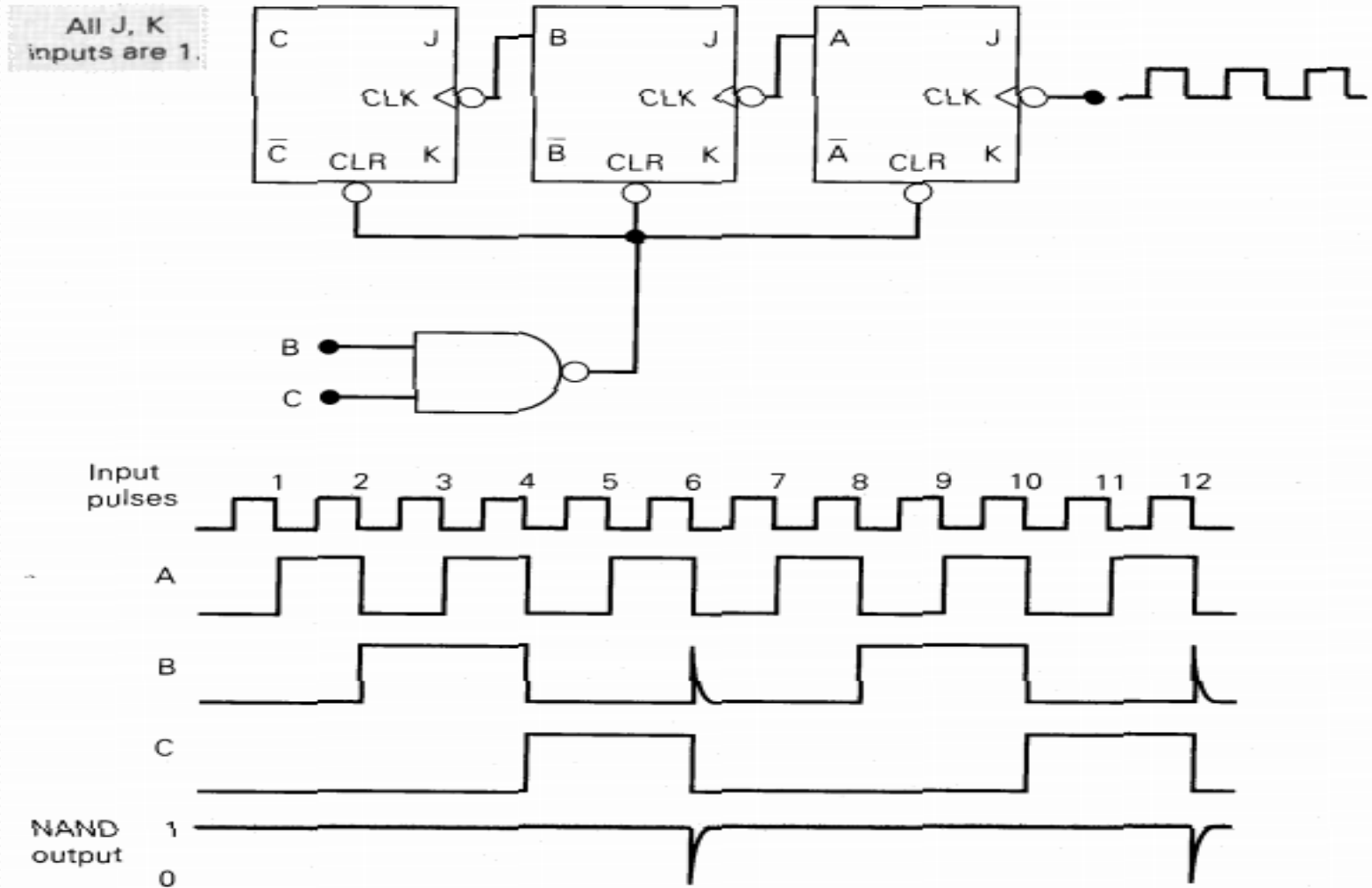


FIGURE 7-3 Example 7-3.

# Asynchronous Counter

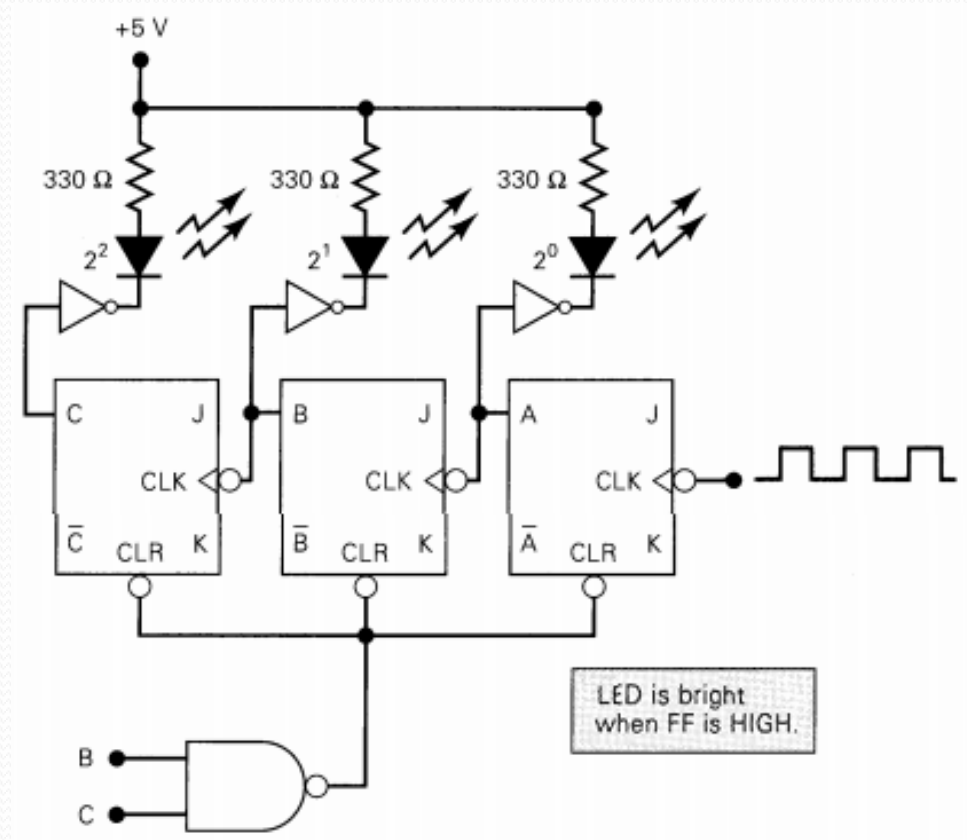
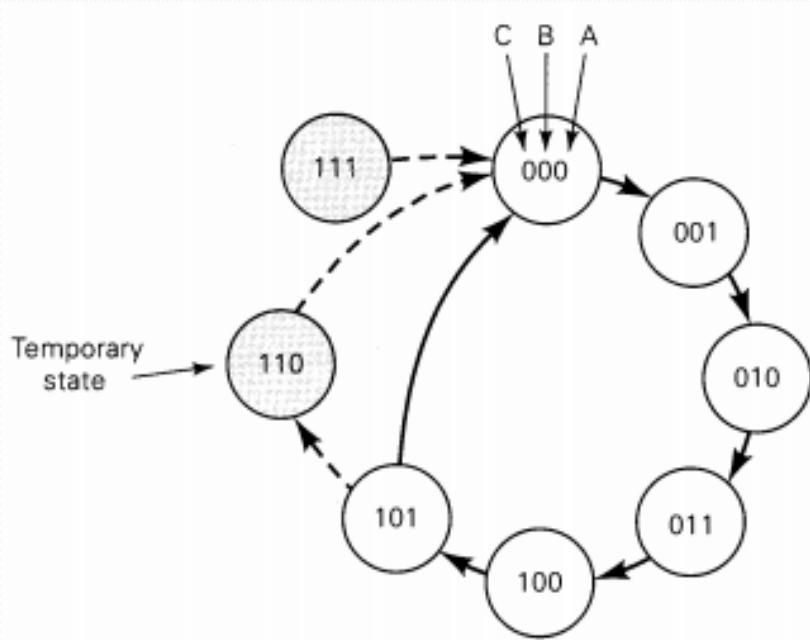
- Counter with MOD number  $< 2^N$



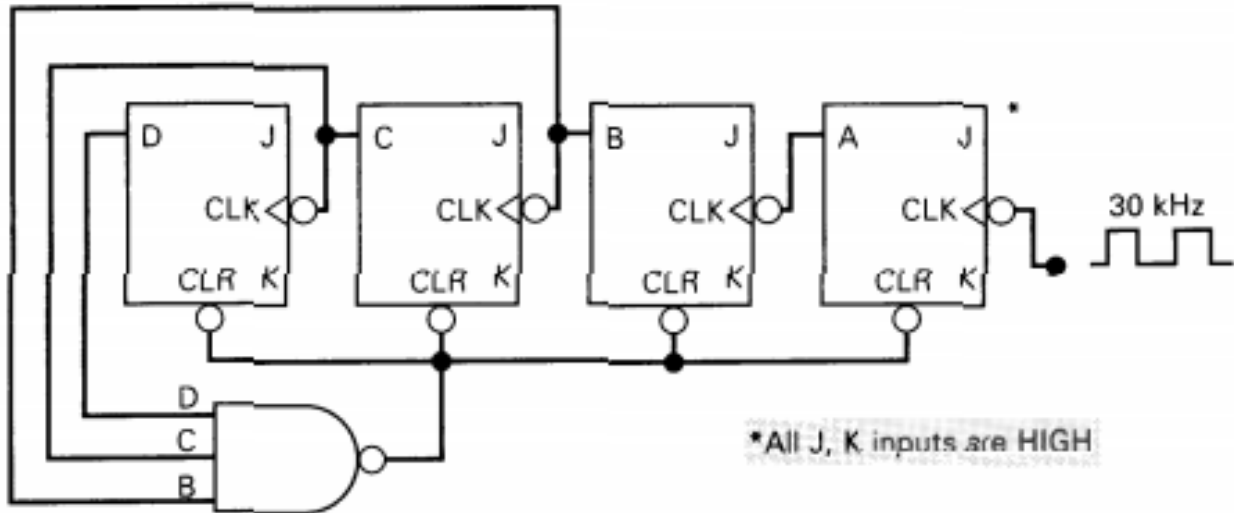


# Asynchronous Counter

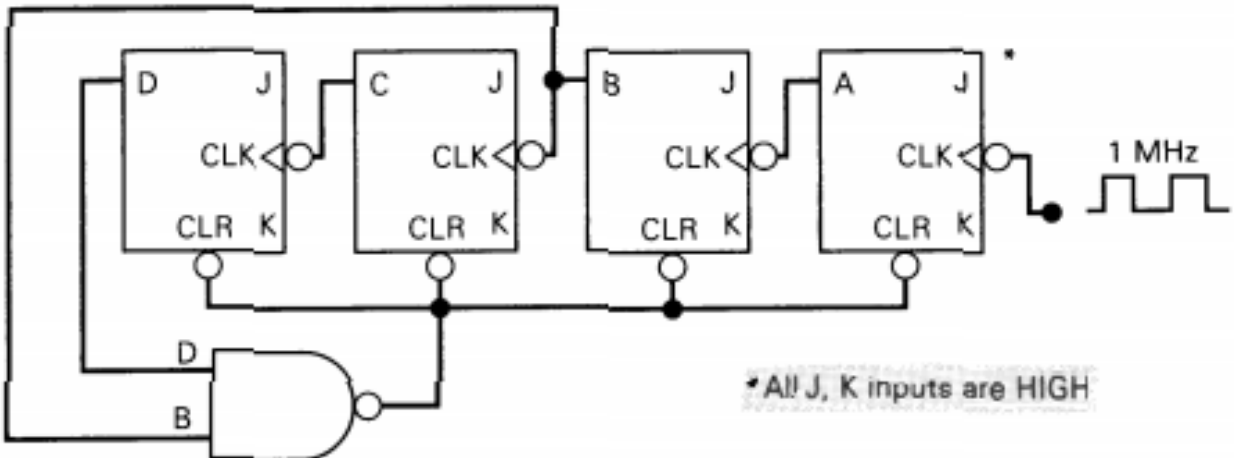
- Counter with MOD number  $< 2^N$



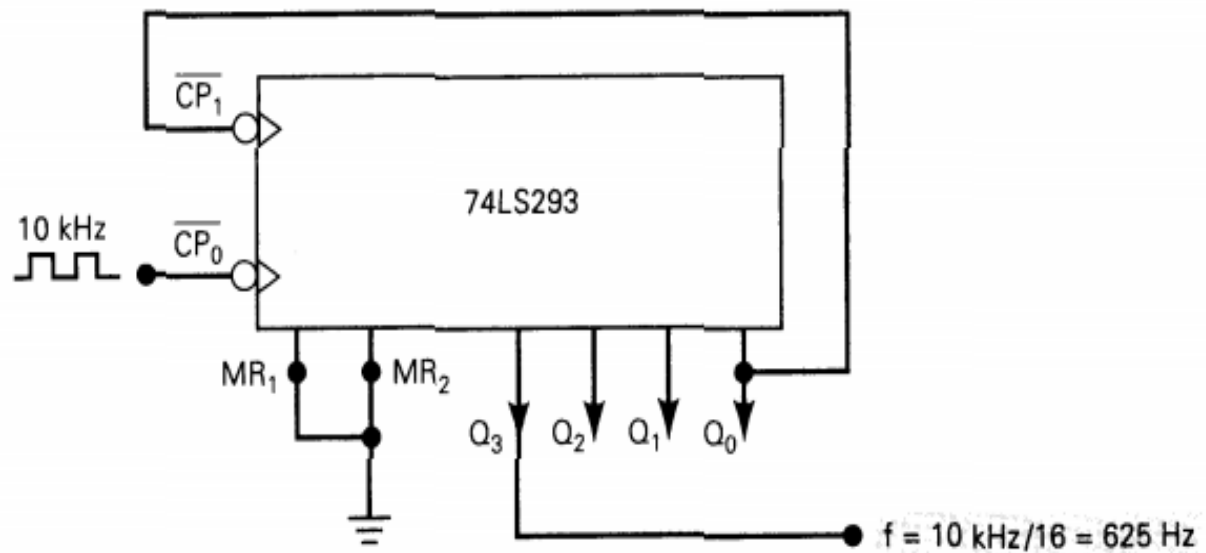
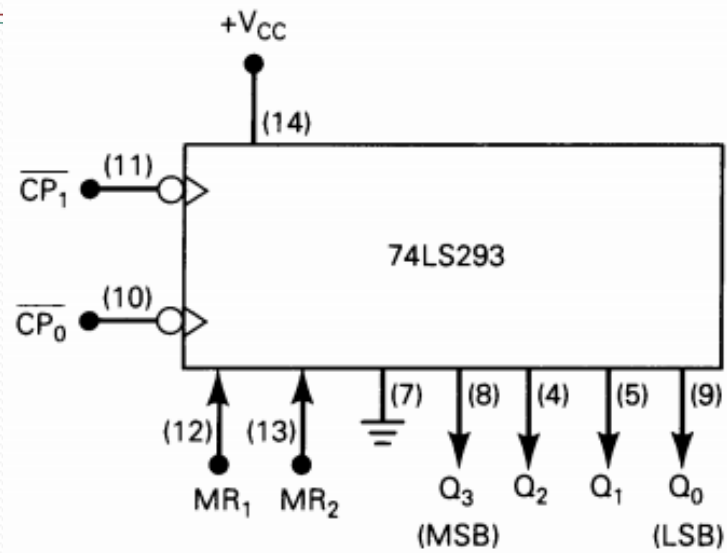
$$\frac{30 \text{ kHz}}{14} = 2.14 \text{ kHz}$$

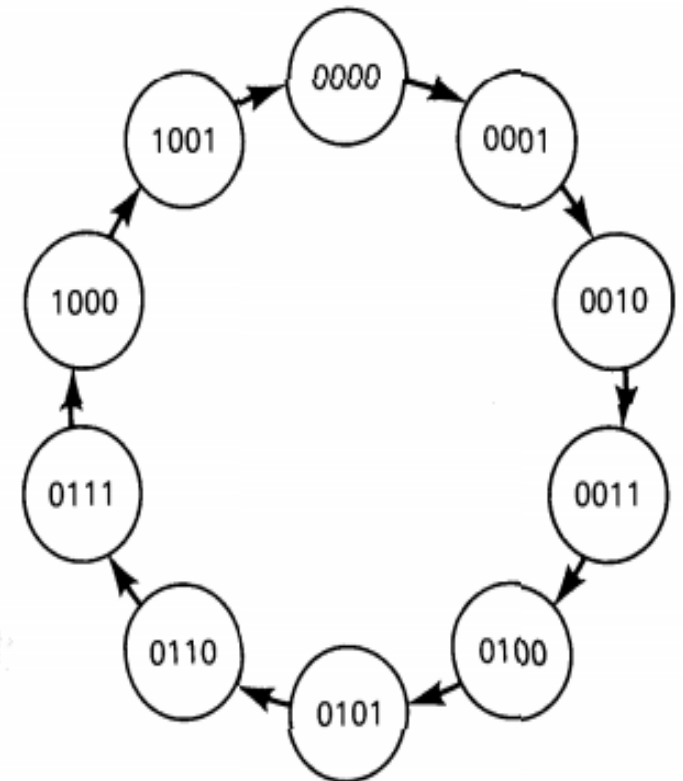
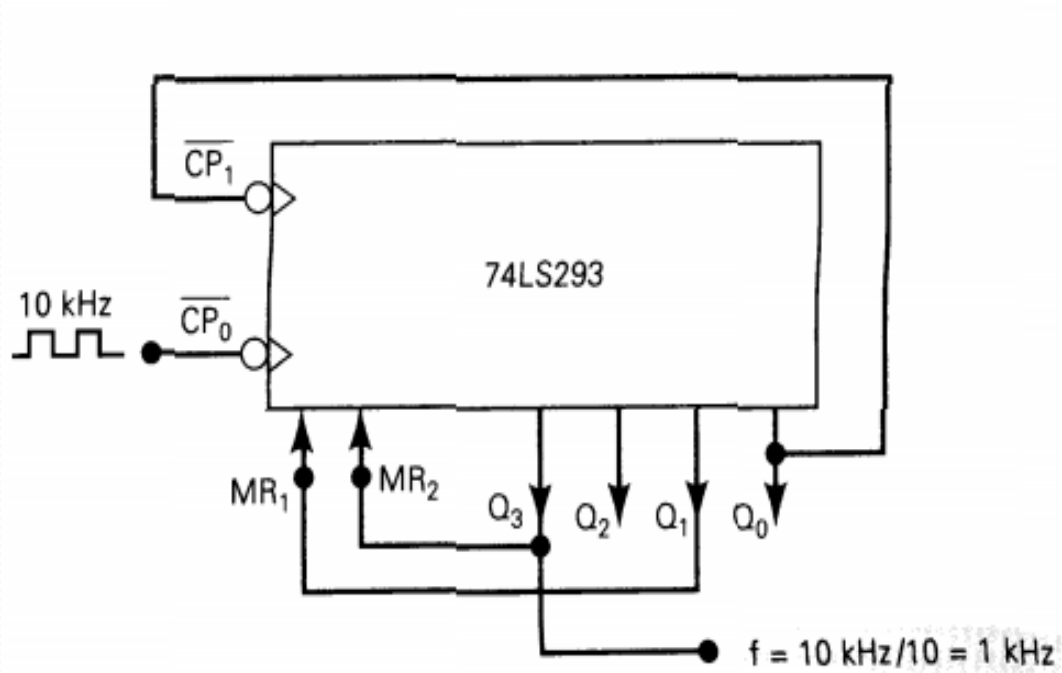


(a)



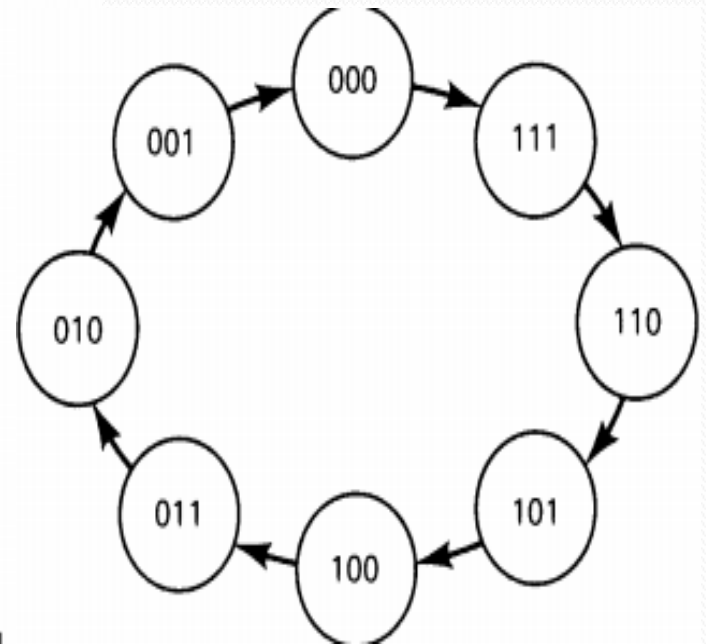
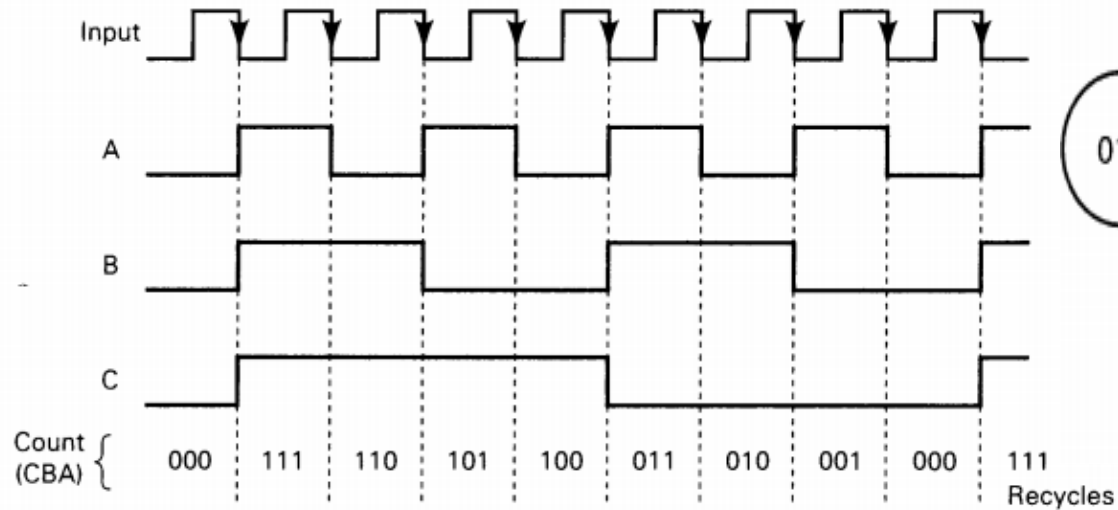
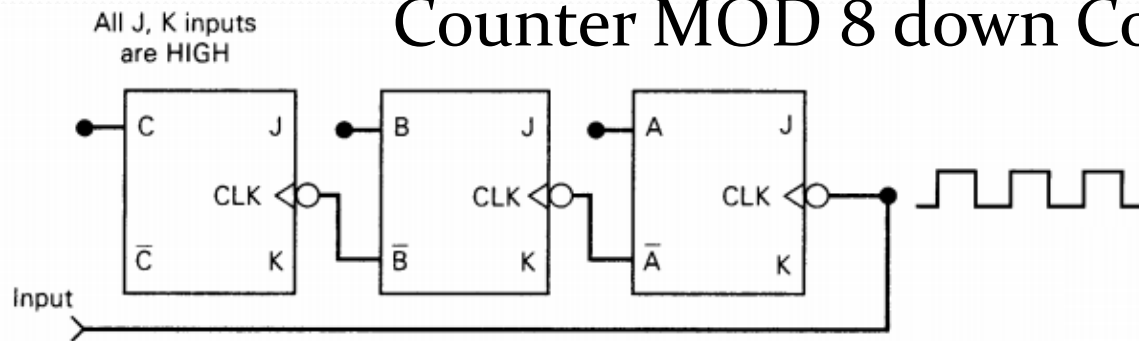
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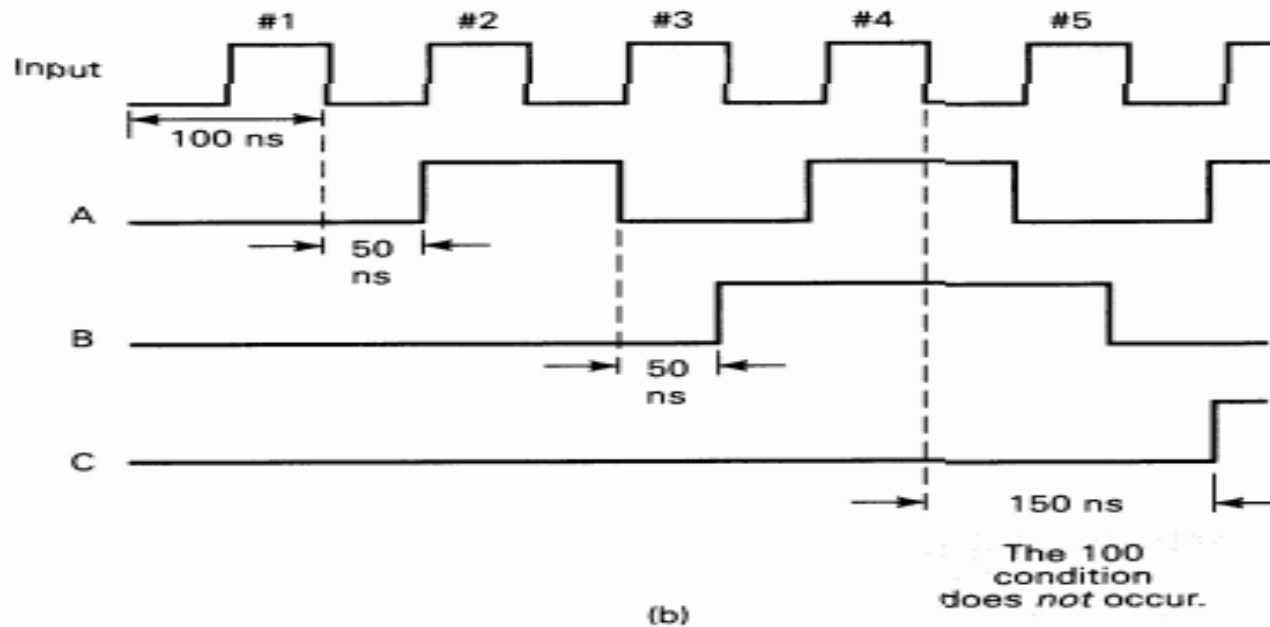
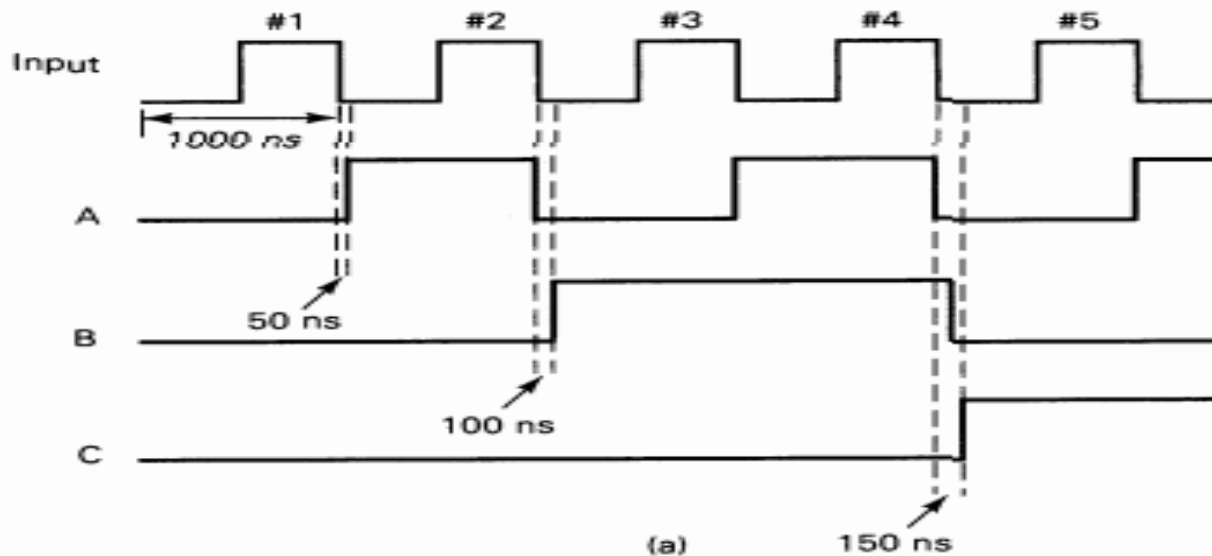


# Asynchronous Counter

## Counter MOD 8 down Counter

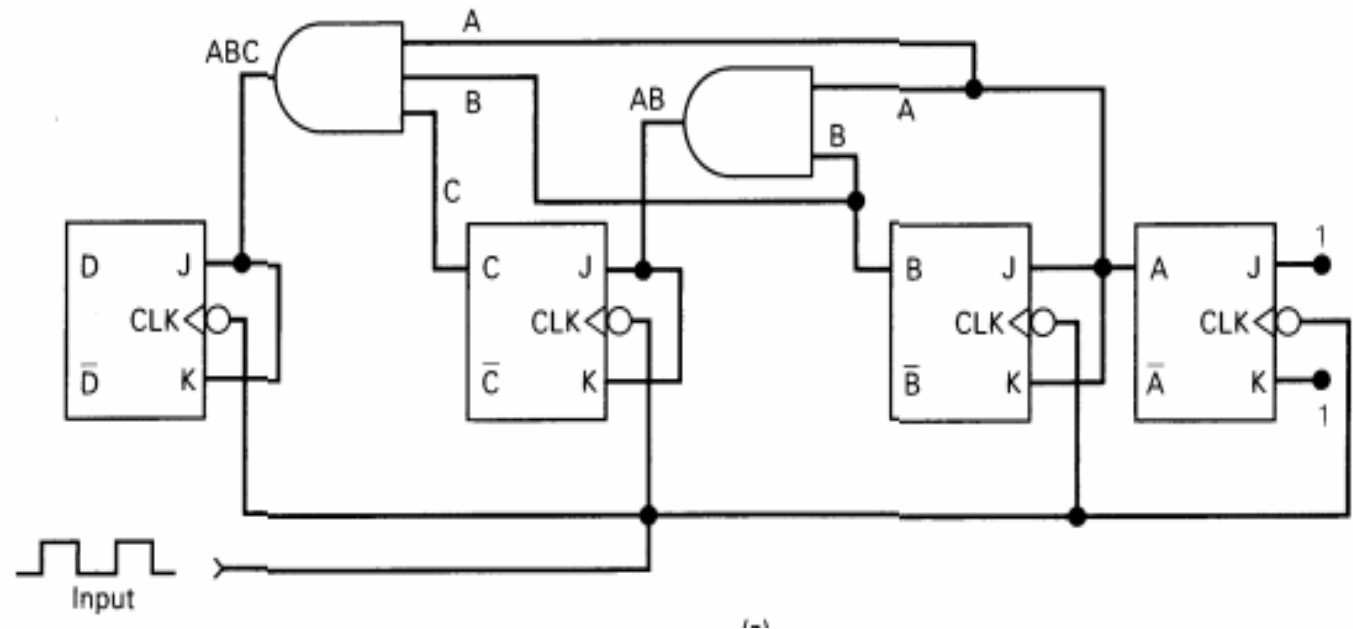


# Delay propagasi



# Synchronous Counter

Count	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
0	0	0	0	0
.	.	.	.	.
.	.	.	.	.
.	.	etc.	.	.



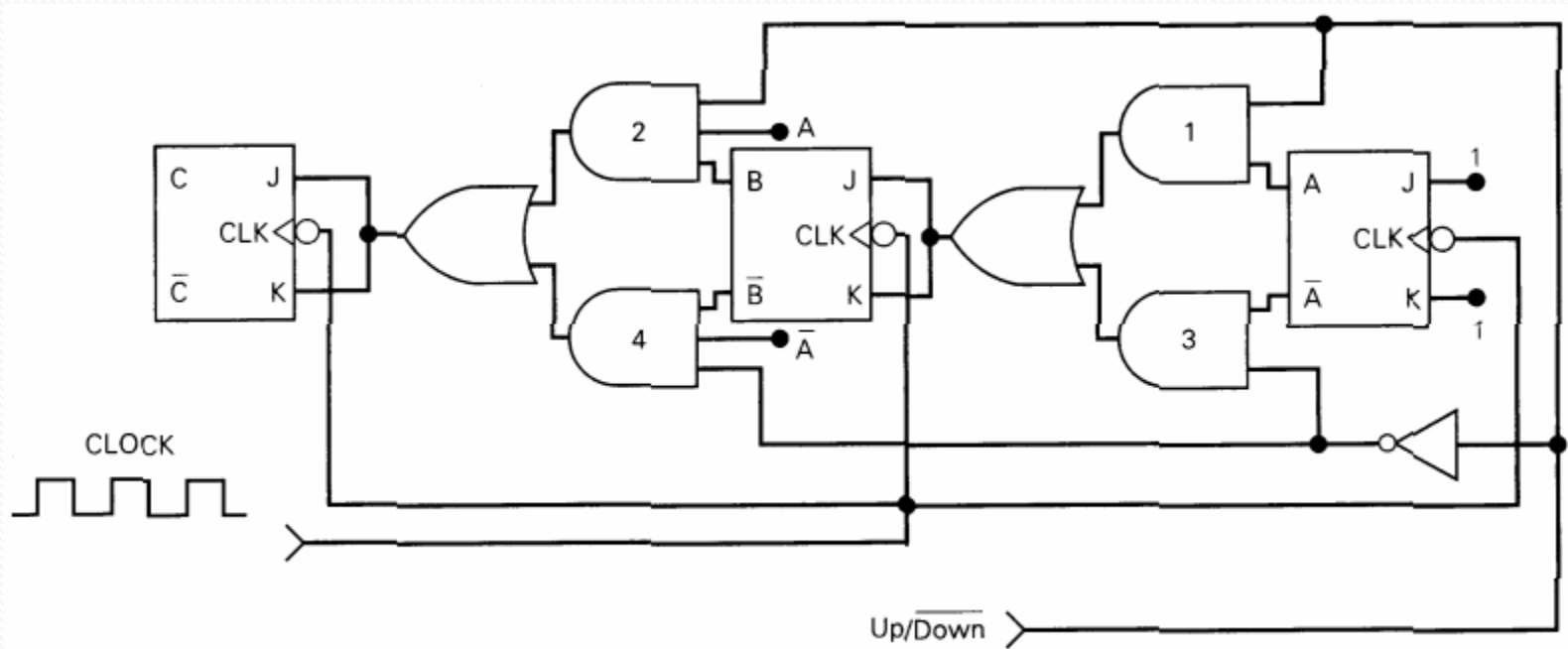
# Synchronous Counter

- Input clock pada semua FF bersumber dari satu clock sumber
- Hanya FF A yang input J dan K nya bernilai 1.
- Adanya rangkaian tambahan



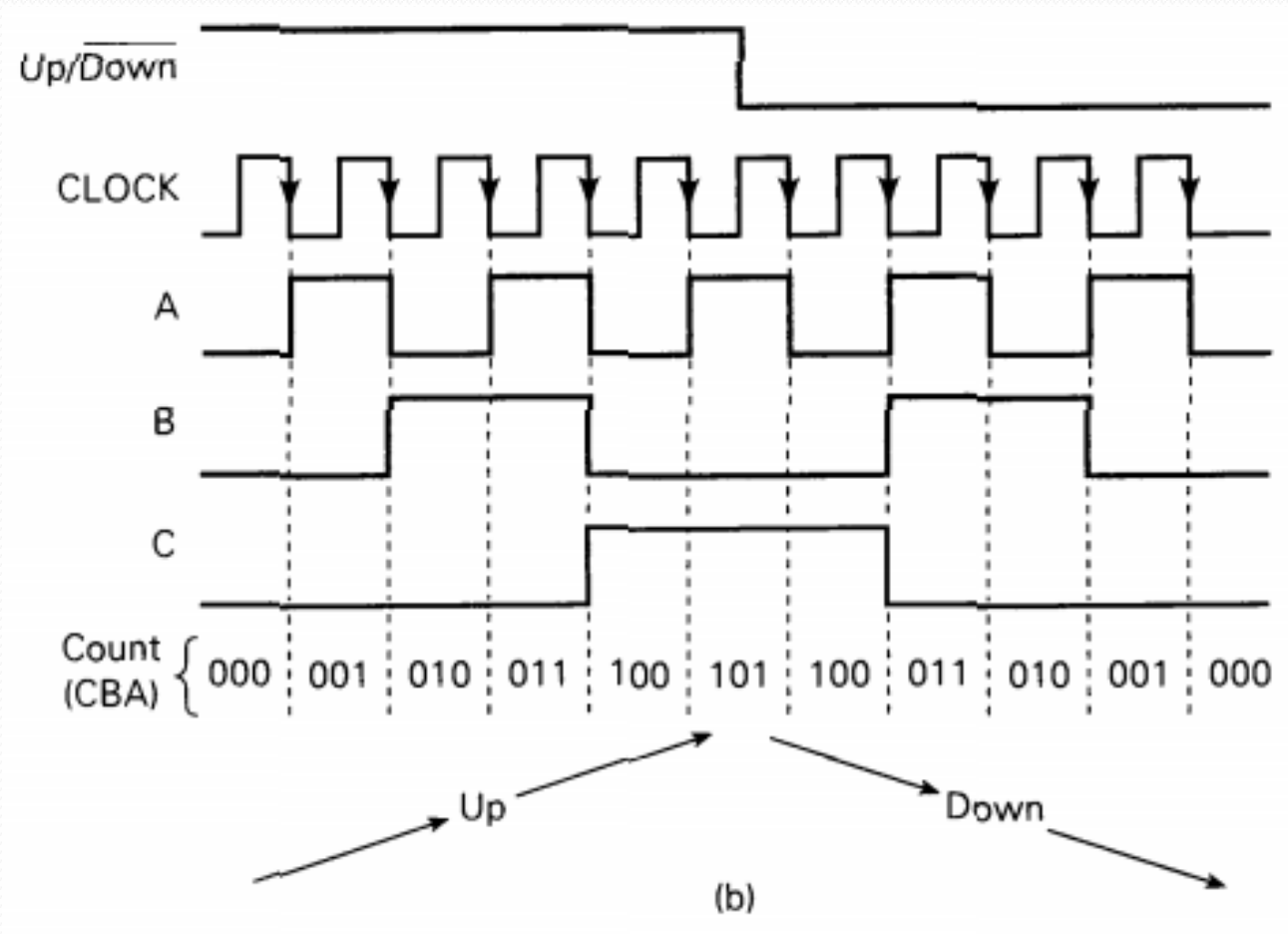
# Synchronous Counter

- Up/Down counter



# Synchronous Counter

- Up/Down counter



# Presetable Counter

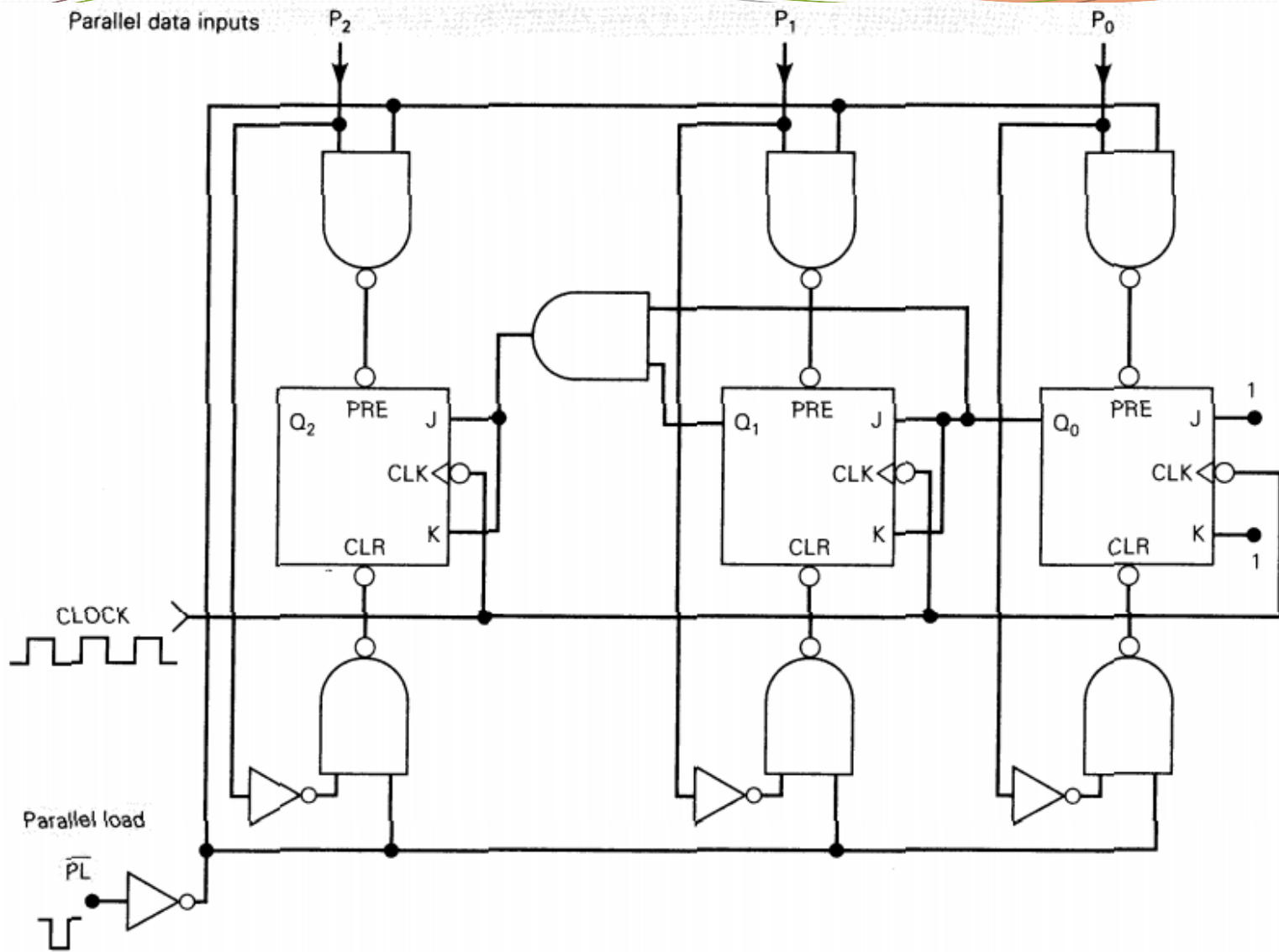
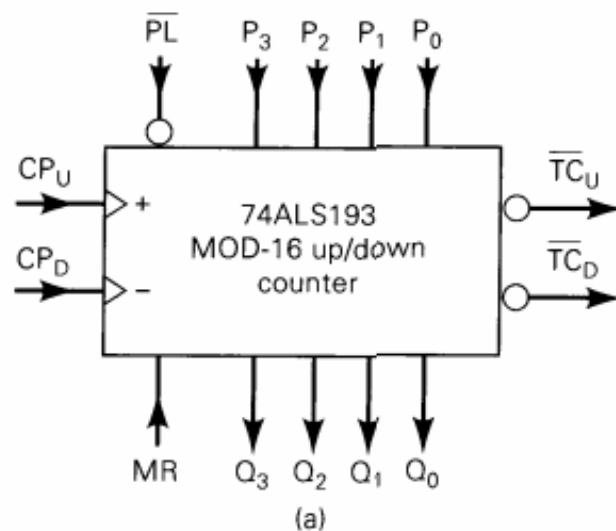


FIGURE 7-19 Presettable parallel counter with asynchronous preset.



Mode Select				
MR	$\overline{\text{PL}}$	CP <sub>U</sub>	CP <sub>D</sub>	Mode
H	X	X	X	Asynch. reset
L	L	X	X	Asynch. preset
L	H	H	H	No change
L	H	↑	H	Count up
L	H	H	↑	Count down

H = HIGH; L = LOW

X = Don't care; ↑ = PGT

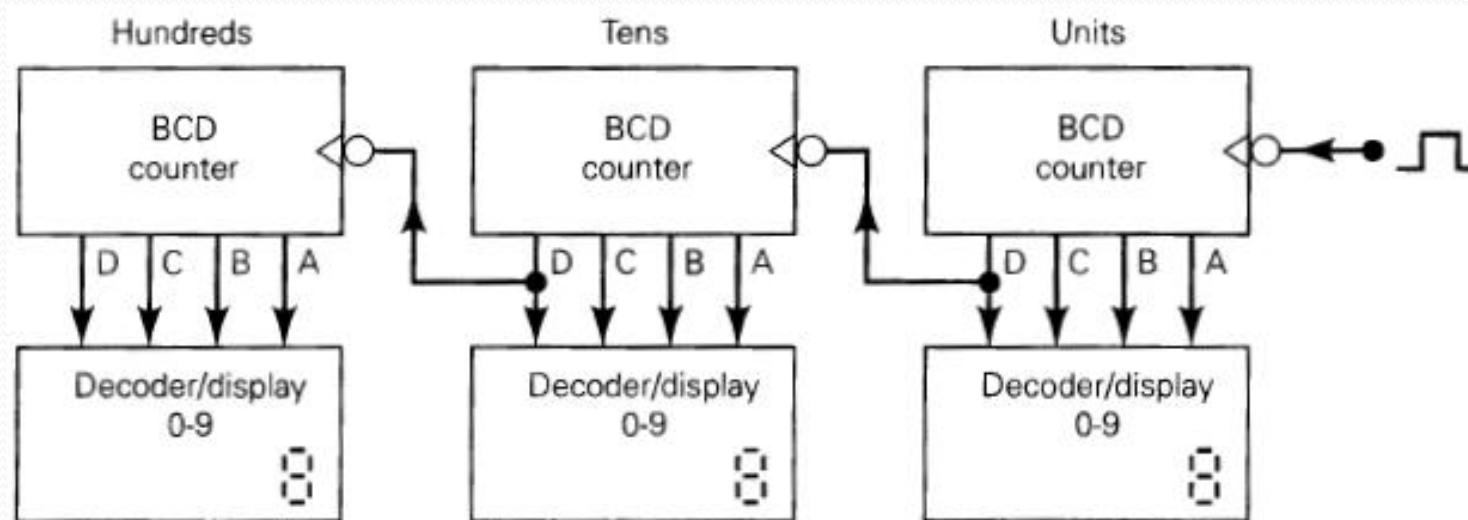
(c)

Pin	Description
CP <sub>U</sub>	Count-up clock input (active rising edge)
CP <sub>D</sub>	Count-down clock input (active rising edge)
MR	Asynchronous master reset input (active HIGH)
$\overline{\text{PL}}$	Asynchronous parallel load input (active LOW)
P <sub>0</sub> -P <sub>3</sub>	Parallel data inputs
Q <sub>0</sub> -Q <sub>3</sub>	Flip-flop outputs
$\overline{\text{TC}}_{\text{D}}$	Terminal count-down (borrow) output (active LOW)
$\overline{\text{TC}}_{\text{U}}$	Terminal count-up (carry) output (active) LOW

(b)

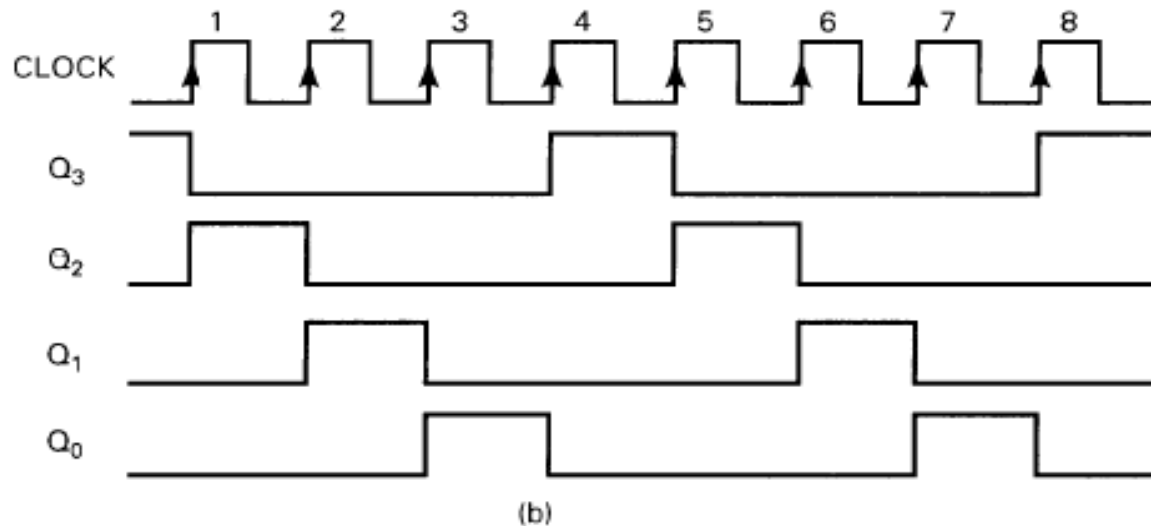
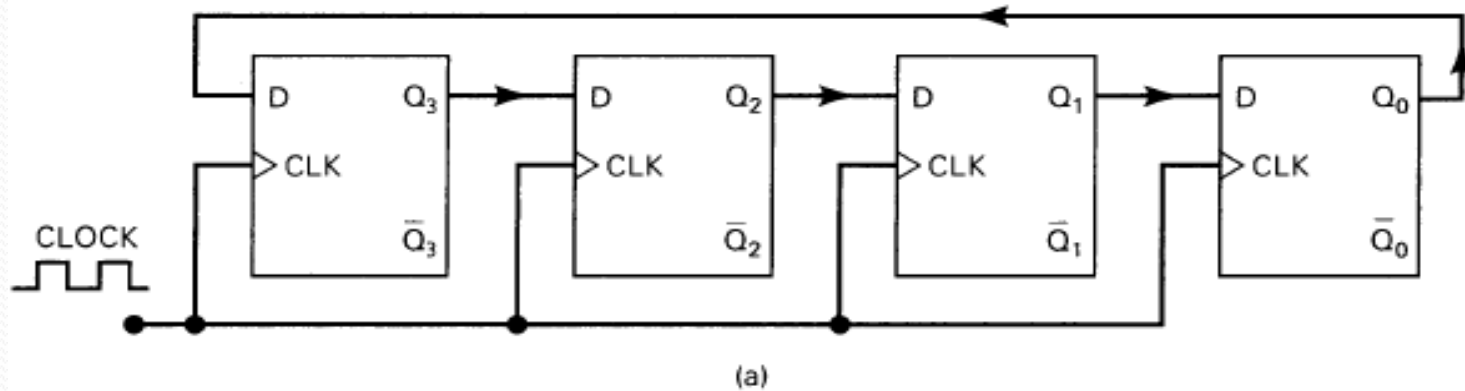
**FIGURE 7-20** 74ALS193 up/down synchronous counter with asynchronous preset and reset: (a) logic symbol; (b) input/output description; (c) mode-select table. (Courtesy of Fairchild, a Schlumberger company)

# BCD Counter



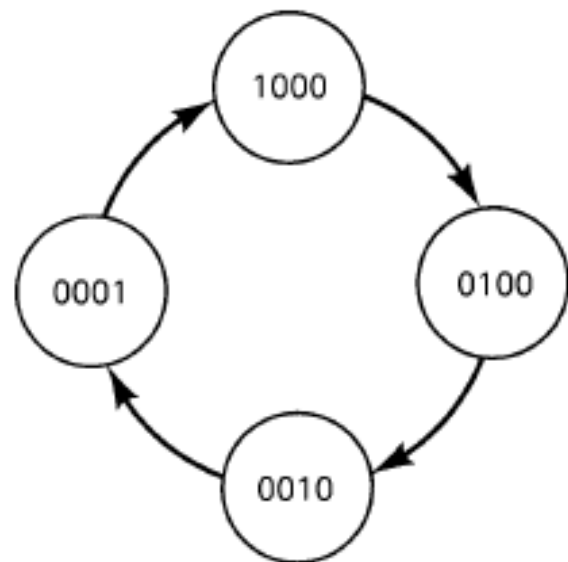
7-32 Cascading BCD counters to count and display numbers from 000 to 999.

# Shift Register Counter

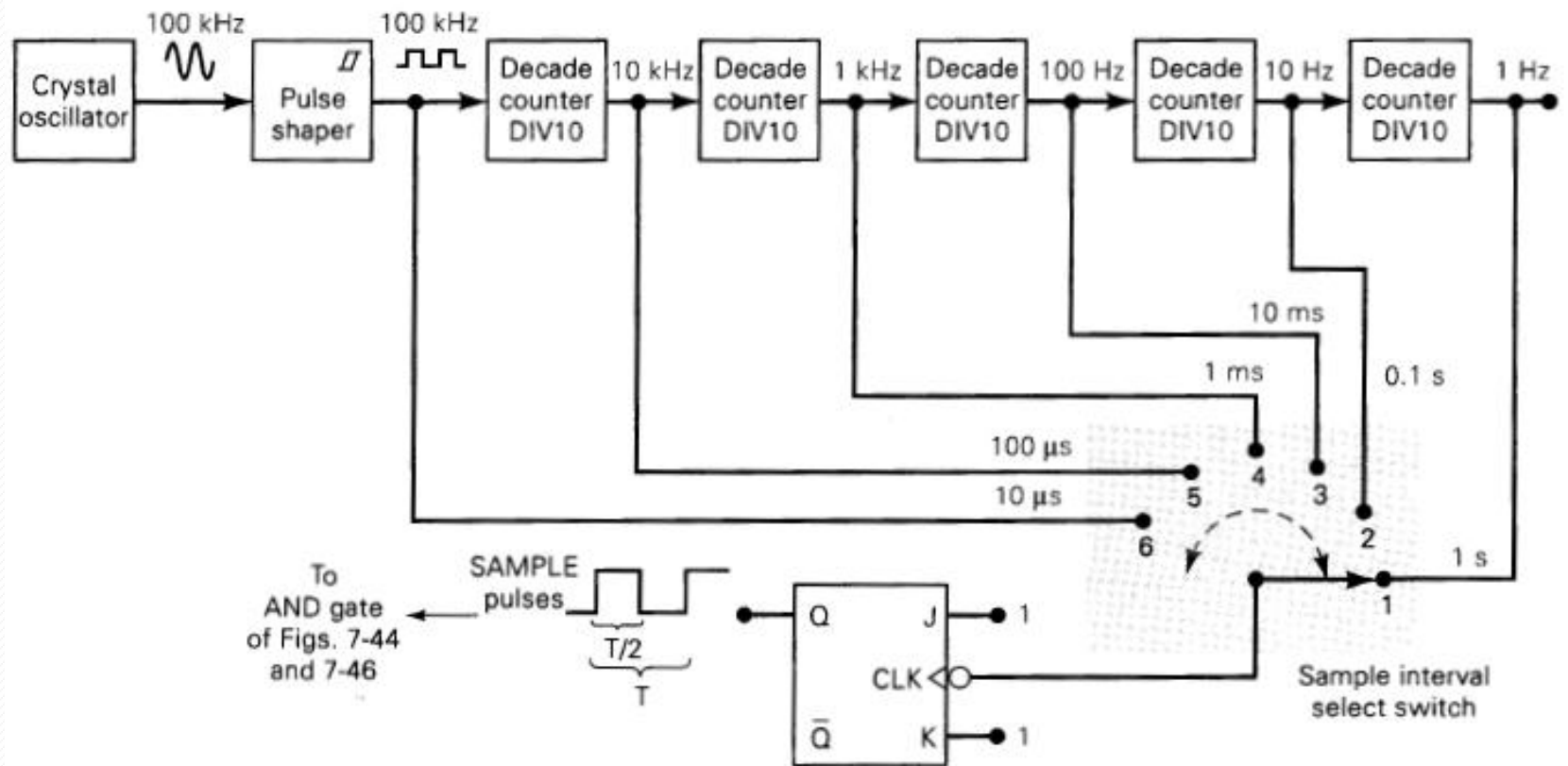


Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>	CLOCK pulse
1	0	0	0	0
0	1	0	0	1
0	0	1	0	2
0	0	0	1	3
1	0	0	0	4
0	1	0	0	5
0	0	1	0	6
0	0	0	1	7
.	.	.	.	.
.	.	.	.	.

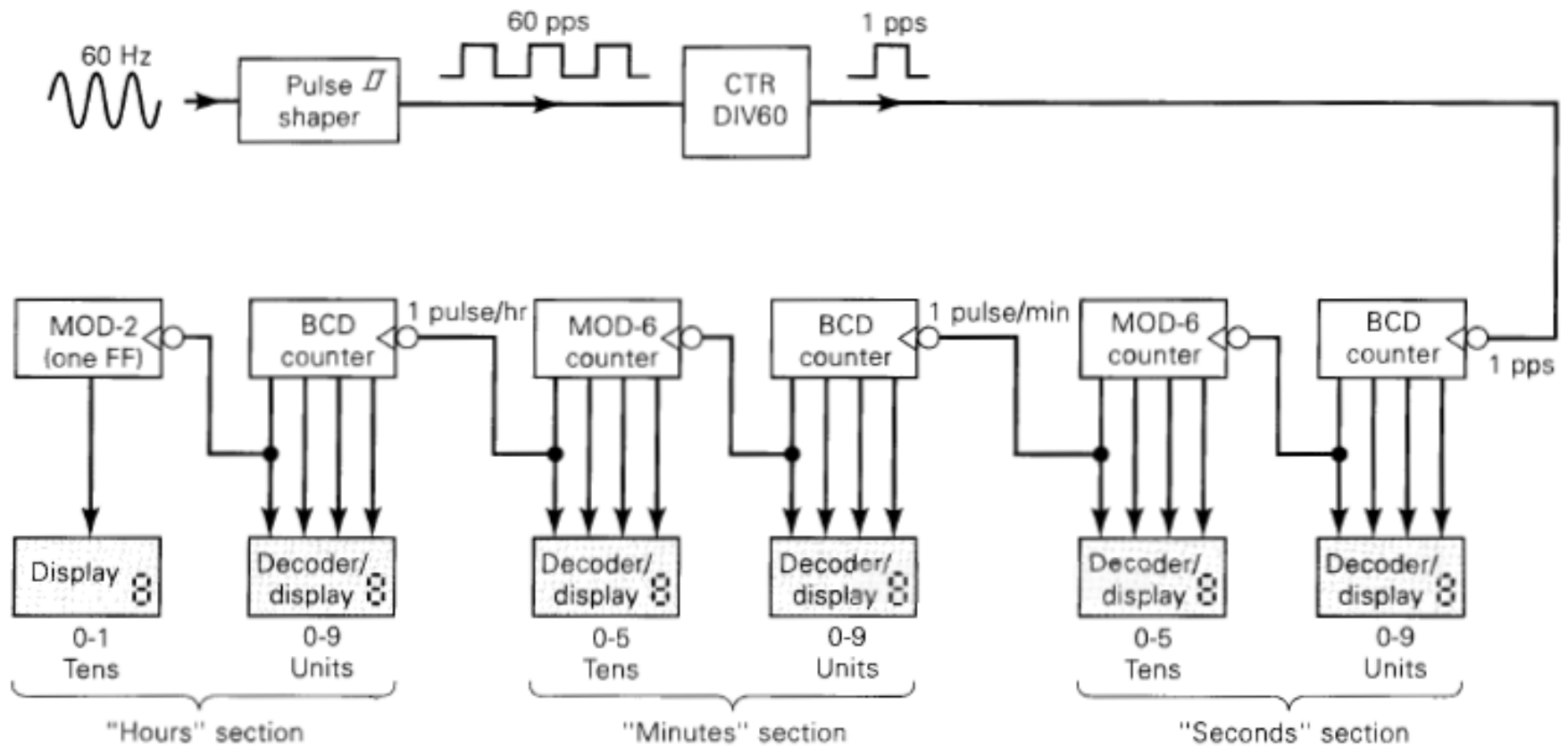
(c)



(d)









**SELESAI**